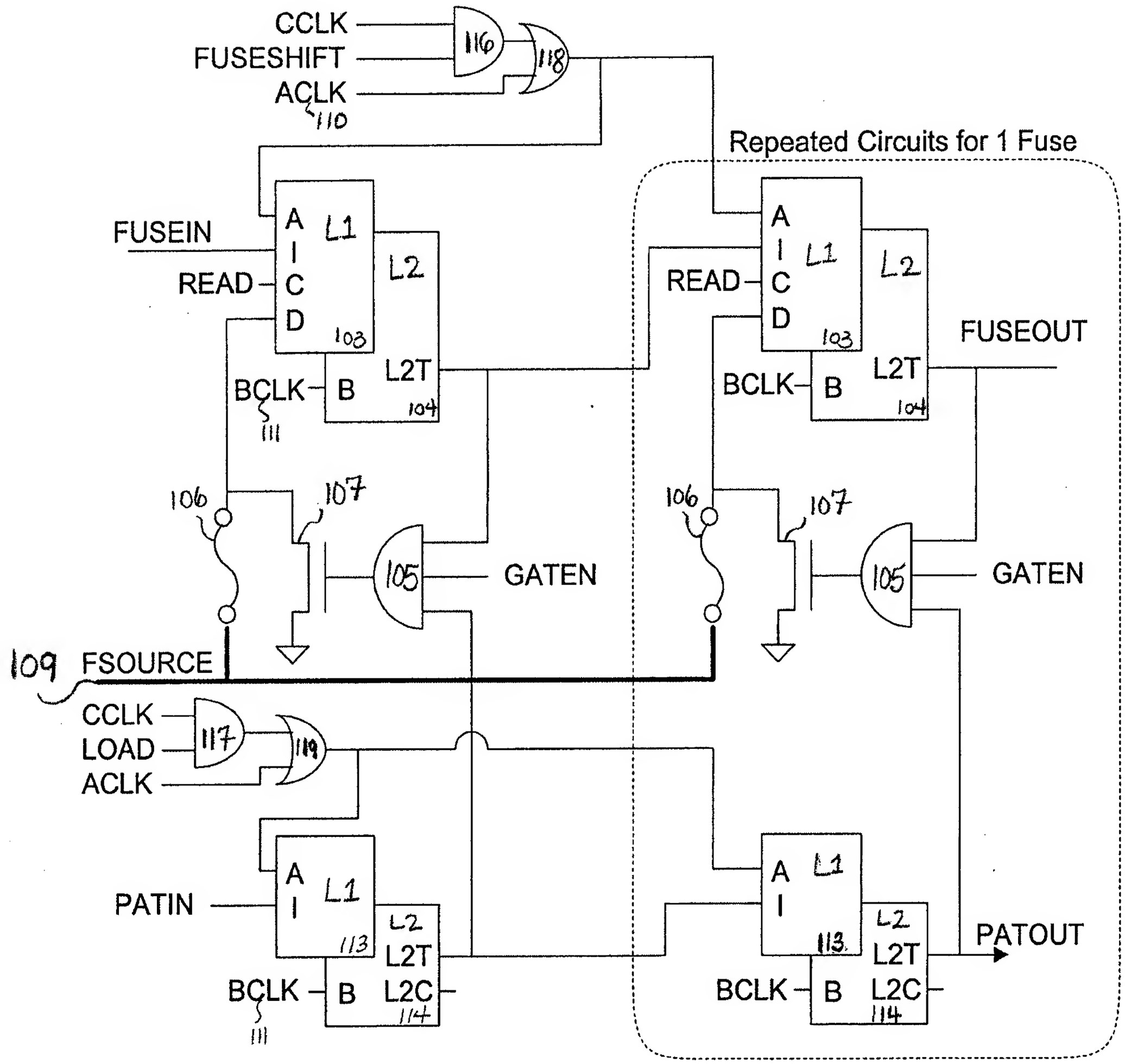

FIG. 1 (PRIOR ART)

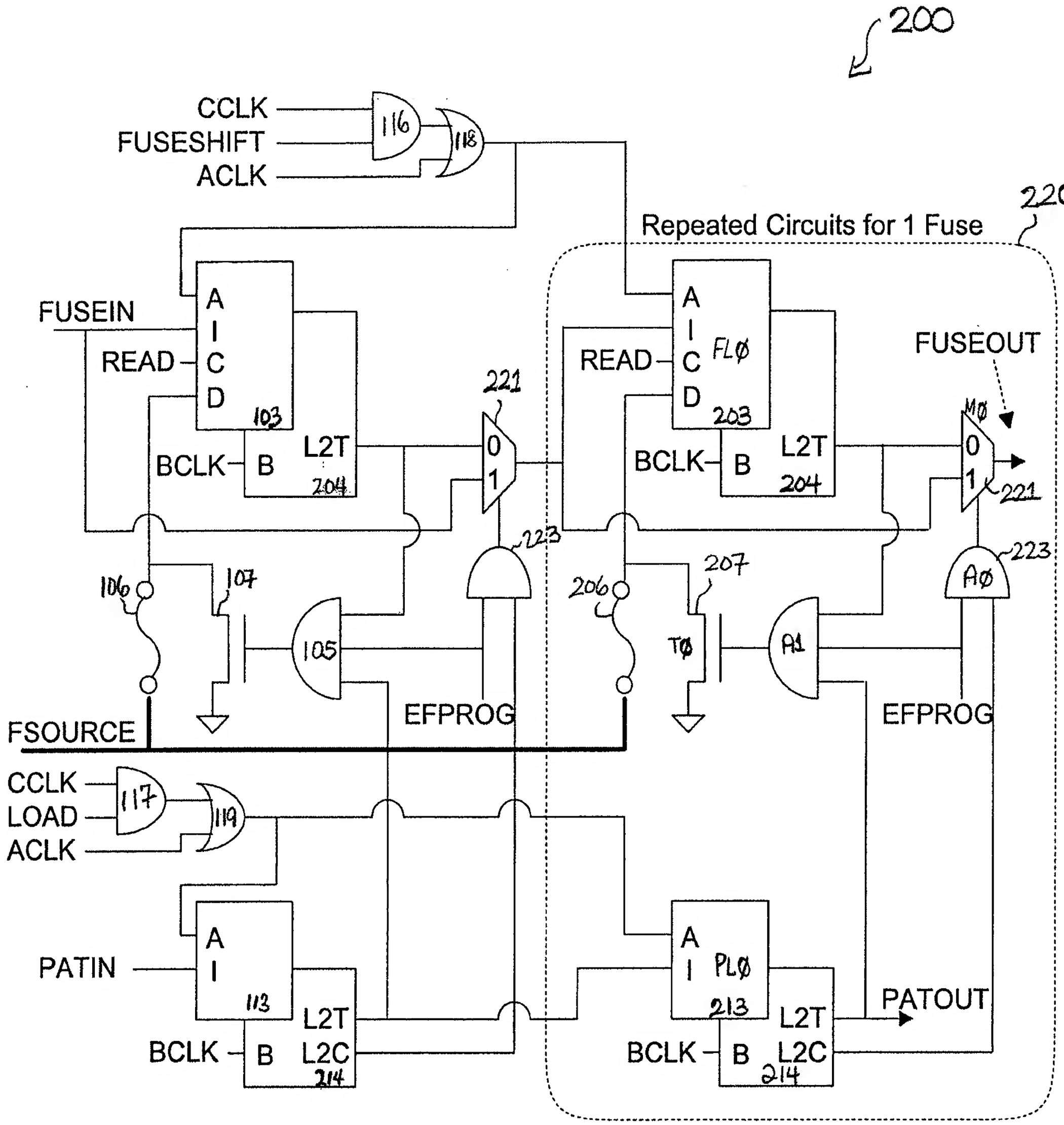
200
CCLK
FUSESHIFT
ACLK
116
118
220
Repeated Circuits for 1 Fuse
FUSEIN
READ
A
I
C
D
103
BCLK
B
L2T
204
221
0
1
223
106
107
105
EFPROG
FSOURCE
FUSEOUT
FLØ
203
MØ
207
206
TØ
A1
AØ
CCLK
LOAD
ACLK
117
119
PATIN
113
L2C
214
PLØ
213
PATOUT

FIG. 2

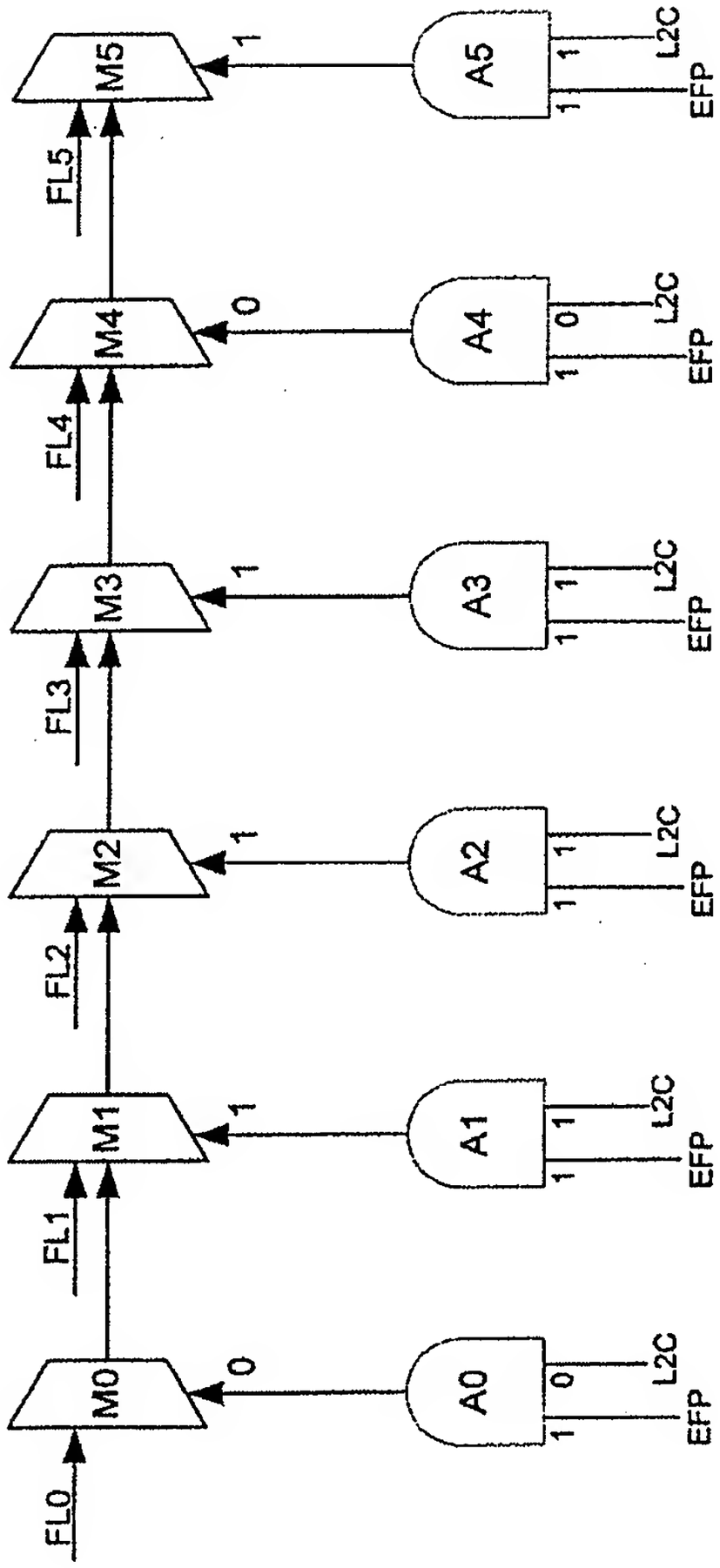

FIGURE 3A

M5	M4	M3	M2	M1	M0	
0	1	0	0	0	1	PRE-PROGRAMMED PATTERN LATCH
MUX	LATCH	MUX	MUX	MUX	LATCH	LOGIC SIGNALED
1	1	1	1	1	1	TEST TIME IN CLOCK CYCLES FOR SERIAL SHIFT (PJA)
.01	1	.01	.01	.01	1	TEST TIME IN CLOCK CYCLES WITH BYPASS

FIGURE 3B

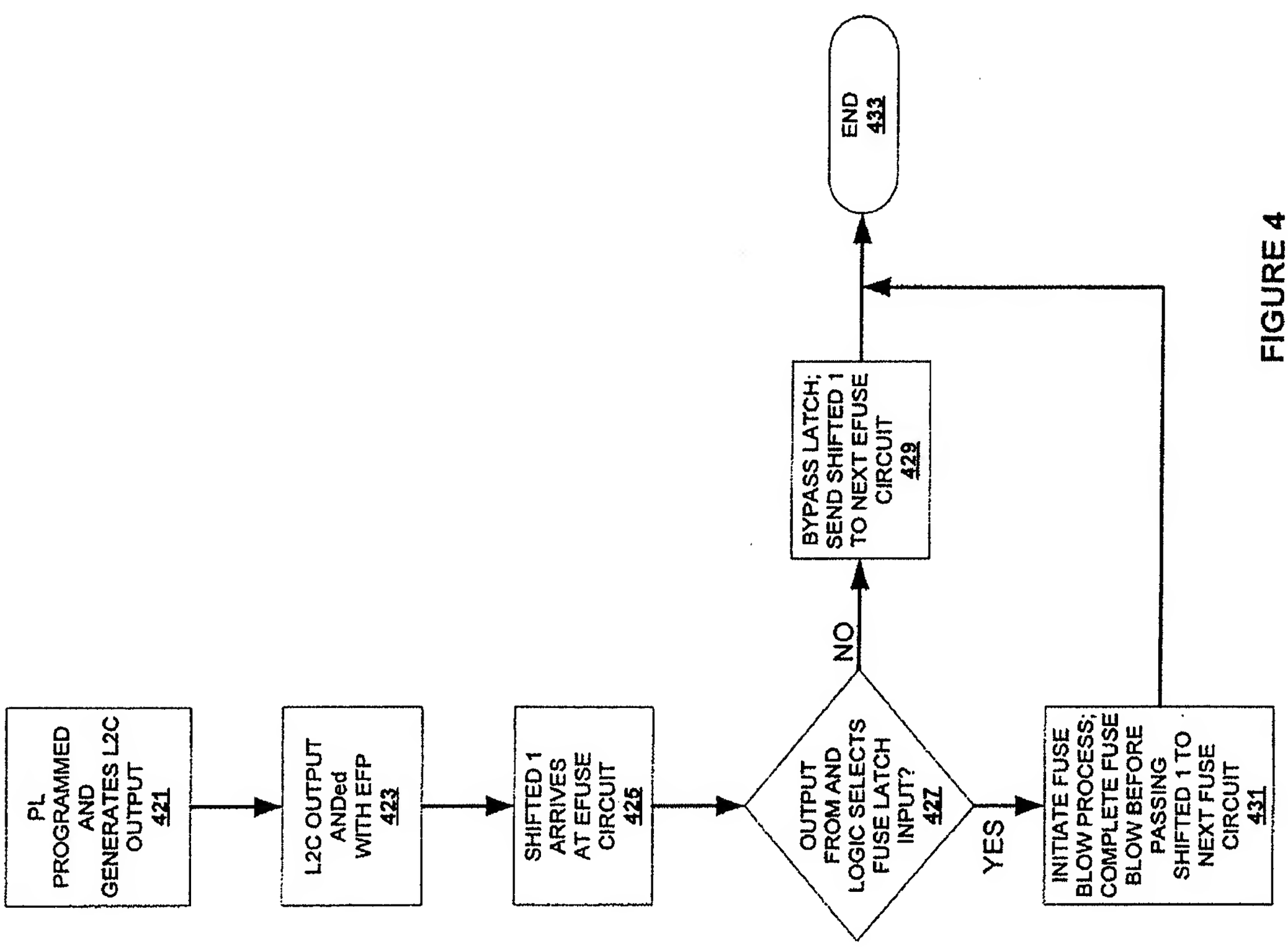
PL PROGRAMMED AND GENERATES L2C OUTPUT 421
L2C OUTPUT ANDed WITH EFP 423
SHIFTED 1 ARRIVES AT EFUSE CIRCUIT 426
OUTPUT FROM AND LOGIC SELECTS FUSE LATCH INPUT? 427
NO
YES
BYPASS LATCH; SEND SHIFTED 1 TO NEXT EFUSE CIRCUIT 429
INITIATE FUSE BLOW PROCESS; COMPLETE FUSE BLOW BEFORE PASSING SHIFTED 1 TO NEXT FUSE CIRCUIT 431
END 433

FIGURE 4